REMARKS

Applicant affirms the provisional election made on December 10, 2002 with traverse to prosecute claims 1-19 and 24-27.

The title has been changed to Stacked Ball Grid Array which is more descriptive of the invention.

The Examiner has rejected claims 1 and 8 under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. Ikeda et al. is directed toward a mounting structure having a package bearing substrate 6 of ceramic material located between a semiconductor package 10 and a wiring board or printed circuit board (PCB) 9. Ikeda discloses a PCB having a TCE of 20 to 30 ppm and substrate 6 having a TCE of about 7 ppm. To avoid problems associated with the different TCE's, underfill 7 is used between substrate 6 and PCB 9 (col 4, lines1-7) in an attempt to fix substrate 6 and PCB 9 firmly together.

Applicant's invention is directed toward a ball grid array mounted circuit and claim 1 (as amended) requires a flexible substrate, that the first solder connections and the second solder connections are shaped to absorb at least a portion of the stress due to differences between the first TCE and the second TCE with the second solder connections free of underfill. In contrast, Ikeda et al. teaches a rigid substrate 6, e.g., ceramic material, pads 15 and pads 16 of substantially the same size (col. 6, l. 20-23) as well as the use of under-fill 7. Ikeda et al teaches away from the principles of the present invention.

The Examiner has rejected claims 2 and 11 under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., as applied to claim 1 and further in view of Jackson. Claim 1 (as amended) includes the requirement that the stress relief substrate be flexible. Jackson discloses an organic interposer 30 preferably FR4, col 3 line 64, and having a thickness preferably in the range of about

1.5 to 3 mm(about 60 to 120 mils), col 3 line 15-16. Applicant submits that FR4 in the preferable thickness disclosed by Jackson would not be flexible and therefore would not meet claim 1. Claim 2 further requires that the polyimide have a thickness in the range of about 2 to 5 mils or more than an order of magnitude difference in thickness than proposed by Jackson.

The Examiner has rejected claim 3 and 4 under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., as applied to claim 1 and further in view of Osaka. Claim1 requires that the first and second solder joints be shaped to absorb at least a portion of the stress due to TCE differences. The Examiner asserts that Osaka discloses comparatively smaller pads on the middle substrate than on the component and board to have better stress control in figure 14. Fig. 14 as well as the discussion relating to an intermediate polyimide film identified at col. 5, line. 47 as "N" and in FIG. 10 as "n" has been reviewed. What is disclosed is a highly complex structure wherein one side of film n includes a pad l' and the other side includes copper l'' with solder e'' extending through film n. Osaka's basic teachings focus strongly on a non-solderable metal layer between the two solderable metals for preventing diffusion. This may be because the solderable layers are quite thin (about 5 micron). The present invention does not teach a diffusion barrier, but rather uses copper metallization for the solder pads, and copper vias through the flexible substrate. The copper is directly solderable, and is thick enough to prevent diffusion through the substrate. In demonstrations of this technology, copper coated with Ni/Au or OSP (organic solder protectant) to preserve the solderability of the copper after room storage is used, but a diffusion barrier or non-solderable metal between the solderable surfaces is not used. Also, the processes that are described in detail by Osaka for the polyimide interposer are fundamentally different than the processes used for fabricating the interposer of Applicant's invention. Applicant's invention uses fairly standard flex substrate processes such as electroplating and plasma etching of vias. Osaka describes (in great

detail) vacuum deposition processes for the thin film metals, wet etch processes for the metal sandwich structure, and a hydrazine wet etch for the polyimide. A hydrazine wet etch is known to be very difficult to control, and damaging to other metals. The plasma etch process for polyimide is much preferred. The structure proposed in Osaki, for example FIG. 11 (12) is not comparable and provides no teaching relative to the structure of Applicant's invention. Further, Jackson teaches the use of underfill 24 to structurally couple substrate 20 to interposer 30 to reduce strain on joints and therefore does not meet the requirement of claim 1 that the second solder connections be free of underfill. Further there is no teaching or suggestion in Ikeda, Jackson or Osaka of deliberately shaping the solder joints by any means. Claims 3 and 4 require selective sizing of pads on the component and the PCB relative to pads on the interposer.

The Examiner has rejected claims 5, 6-7, 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. Claim 5 requires the connection pads to capture a plurality of conductive vias and Ikeda does not teach or suggest this feature. Claims 6-7 specify size and other characteristics of vias and connection pads and Ikeda provides no teaching of these features. Claims 9 and 10 require that the electronic component be a chip scale package and a ruggedized die respectively and Ikeda et al provides no teaching relative to these devices.

The Examiner has rejected claims 12-19 and 24-27 under 35 U.S.C. 103(a) as being unpatentable over the combination of Ikeda et al, Jackson et al as applied to claims 1-11. Claim 12 specifically requires the component connection pad to be larger than the pad at the upper surface of the flexible substrate and the PCB pad to be larger than the pad at the lower surface of the flexible substrate and that the connections formed between the component and the PCB have an hourglass shape to absorb at least a portion of the stress due to TCE differences. Ikeda and Jackson provide

no teaching or suggestion of these required features. Other features of claims 12 and 24 have been discussed with regard to the response to the rejection of claim 1 as discussed above.

Claim 13 includes limitations similar to claim 2.

Claim 14 includes limitations similar to claim 5.

Claim 15 includes limitations similar to claim 6.

Claim 16 includes limitations similar to claim 7.

Claim 17 includes limitations similar to claim 8. The response to the rejections of claims 2, and 5-8 are discussed above. Claims 18 and 19 are believed to be allowable at least for the reason that they depend on allowable claim 12.

Claim 24 requires specific relationships of connection cross sectional areas and that the combination of the first connections and the second connections have hour glass shapes and are sufficiently compliant to absorb at least a portion of the stress due to TCE differences. These features are not taught by the references. Claims 25, 26 and 27 include limitations similar to claims 2, 6, and 7 respectively and the response to the rejection of these claims has been provided above.

Therefore, since the claims of the present invention have been shown to include limitations not taught or suggested by the references cited, the Examiner is requested to allow claims 1-19 and 24-27 and to pass this application to issue.

Respectfully submitted,

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